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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,319	11/24/2003	Hong-Gun Kim	5649-1182	9100
20792	7590	11/30/2005	EXAMINER	
MYERS BIGEL SIBLEY & SAJOVEC			GOUDREAU, GEORGE A	
PO BOX 37428			ART UNIT	
RALEIGH, NC 27627			PAPER NUMBER	
			1763	
DATE MAILED: 11/30/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

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1. Applicant's arguments with respect to claims of record have been considered but are moot in view of the new ground(s) of rejection.

-Applicant should note, however, that their claims are not commensurate in scope with any showing of unexpected results based upon applicant's previous arguments of record. Applicant previously argued unexpected results occur for a temperature range of (150-350) C. Applicant then claims temperatures, which fall outside this range, which would be prima facie obvious. Thus, applicant is not entitled to any claim of unexpected results based upon their claims as presently claimed.

2. This action will not be made final due to the new grounds of rejection.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 15, 17, 19-21, 31, 33-36, and 38-39 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Hong et. al. (6,566,229).

Hong et. al. discloses a process for fabricating a STI structure on the surface of a wafer (10) which is comprised of the following steps:

-A Si₃N₄ layer (13)/ pad SiO₂ layer (11) is formed onto the surface of a

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wafer (10).;

-A patterned photo resist etch mask is used in the patterning of an STI trench.;

-A thermal oxide liner (15) is formed inside the STI trench.;

-A Si₃N₄ liner layer (17) is conformably formed onto the surface of the wafer as well as inside the STI trench.;

-A SOG, polysilazane layer (21) is then conformably formed inside the STI trench using a spin coating process.;

-The SOG layer is soft baked a temperature of (100-300) C.;

-The SOG layer is hard baked at a temperature of 400 C.;

-The SOG layer may be recessed (i.e.-wet etched) using a solution comprised of (HF-NH₄OH) at this point. Alternatively, the wet etching process may occur after the SOG layer is annealed to form SiO₂.;

-A SiO₂ layer (31) is then CVD deposited onto the surface of the wafer.;

-The SOG layer is then thermally annealed at a temperature of (700-800) to form SiO₂.;

-The SiO₂ layer is then cmp polished down to the surface of the Si₃N₄ polish stop layer (13).; and

-The Si₃N₄ layer (13), and SiO₂ pad layer (11) are then removed from the surface of the wafer.

This is discussed specifically in columns 1-5; and discussed in general in columns 1-8. This is shown in figures 1-5.

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5. Claims 15-17, 20-21, 31, 34-36, and 38-39 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Hideaki (JP 2000-114,362).

Hideaki discloses a process for forming a STI structure on the surface of a wafer, which is comprised of the following steps:

-A Si₃N₄ pad layer (3)/ SiO₂ pad layer (2) is formed onto the surface of a Si wafer.;

-An STI trench etched through the pad layers, and into the surface of the Si wafer.;

-A SiO₂ liner layer (4) is formed inside the STI trench.;

-A HSQ SOG layer (5) is used to fill the STI trench in the Si wafer.;

-The SOG layer is baked at a temperature of 400 C (i.e.-about 300 C).;

-The SOG is dry etched to form a recess at the top of the STI trench.;

-A HTO oxide layer is formed at 800 C using a CVD process. (This thermal CVD process would inherently anneal the previously deposited SOG layer at a temperature of 800 C in the process for forming the HTO oxide layer.);

-The HTO oxide layer is cmp polished down to the Si₃N₄ polish stop layer.; and

-The Si₃N₄ pad layer, and the SiO₂ pad layer are removed from the surface of the wafer.

This is discussed specifically in the abstract; and discussed in general on pages 1-3. This is shown in figures 1-5.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

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7. Any inquiry concerning this communication should be directed to examiner

George A. Goudreau at telephone number (571)-272-1434.


George A. Goudreau
Primary Examiner
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